Zirconium oxide-aluminum oxide nanolaminate gate dielectrics for amorphous oxide semiconductor thin-film transistors

T. Waggoner, J. Triska, K. Hoshino, J. F. Wager, and J. F. Conley, Jr.[a)]
Oregon State University, School of EECS, 1148 Kelley Engineering Center, Corvallis, Oregon 97331-5501

(Received 18 February 2011; accepted 1 June 2011; published 10 August 2011)

The dielectric properties of $ZrO_2-Al_2O_3$ nanolaminates, deposited via atomic layer deposition, and their impact on the performance and stability of indium gallium zinc oxide and zinc tin oxide amorphous oxide semiconductor thin-film transistors (TFTs) are investigated. It is found that nanolaminate dielectrics can combine the advantages of constituent dielectrics and produce TFTs with improved performance and stability compared to single layer gate dielectrics. It is also found that TFT performance and stability are influenced not only by the chemical composition of the gate dielectric/channel interface but also by the thickness and composition of the laminate layers in the dielectric near the interface. © *2011 American Vacuum Society.* [DOI: 10.1116/1.3609254]

I. INTRODUCTION

Thin film transistors (TFTs) fabricated using amorphous oxide semiconductors (AOSs) are transparent, exhibit good electron mobility (in the general range of $1-30$ cm^2/V s), and can be processed at low temperature.[1–8] This new class of materials shows promise for application in active-matrix organic light-emitting diode (AMOLED) displays,[9–11] large-area, high-performance active-matrix liquid crystal displays[12] (AMLCDs), and e-paper.[13] Commercialization of these applications will require optimization of TFT performance and reliability.[14–22] It is well known that the performance and stability of field-effect devices such as TFTs depends critically on the gate dielectric and its interface with the active channel and it has been shown recently that a thin dielectric interfacial layer can dominate AOS TFT stability.[20–22] The use of multilayer or nanolaminate gate dielectrics can allow for independent tuning of the properties of the dielectric/channel interface and bulk dielectric.

Atomic layer deposition (ALD) is a highly conformal and uniform technique with inherent atomic-scale control of thin film composition, making it ideally suited for deposition of nanolaminates.[23,24] Previous work has shown that ALD nanolaminates can exhibit superior performance to single layer gate dielectrics in metal/oxide/silicon (MOS) structures[25–30] and perform well as passivation and diffusion barriers for AOS TFTs.[31] Very little work has been reported on the use of ALD nanolaminates as AOS TFT gate dielectrics. Although ALD nanolaminates of $Al_2O_3-TiO_2$ (ATO), typically supplied by Planar Systems, have been used as gate dielectrics for AOS TFTs, there is little information reported about the material.[32,33] Most ATO work in literature has focused on dielectric characterization for use in MOS technologies.[29,34–36]

In this work, we use ALD to deposit $ZrO_2-Al_2O_3$ (ZAO) nanolaminates of various structure, composition, and surface termination at the AOS channel interface and investigate their impact on the performance and stability of TFTs made using two of the most promising AOS materials, zinc tin oxide (ZTO), and indium gallium zinc oxide (IGZO). We find that ZAO nanolaminate dielectrics can be tuned to combine the bulk advantages of the constituent dielectrics—the high dielectric constant of ZrO_2 and the low leakage of Al_2O_3. By using the proper nanolaminate bilayer structure, interfacial material, and thickness/composition of the near-interfacial layers, we were able to improve overall performance compared to TFTs made using single layer films of either Al_2O_3 or ZrO_2.

II. EXPERIMENT

A. Device fabrication

A schematic cross section of the staggered, bottom-gate (SBG) AOS TFTs used in this study is shown in Fig. 1. A heavily doped (0.05 Ω cm) *p*-type Si substrate served as a bottom-gate contact. 25×25 mm^2 *p*-type Si coupons were cleaned with consecutive rinses of acetone, isopropyl alcohol, and 18 M Ω cm de-ionized water, followed by dehydration in an oven at 125 °C for 15 min. Immediately following this procedure, the gate dielectric was deposited via thermal ALD using a Picosun Sunale R-150 reactor. ZrO_2 was deposited at 250 °C using alternating pulses of tetrakis(ethylmethylamido)zirconium (TEMAZ) and H_2O. Al_2O_3 was deposited at 250 °C using trimethylaluminum (TMA) and H_2O. ZAO nanolaminates were deposited at 250 °C in a single ALD run. ZAO nanolaminates are composed of alternating pairs of ZrO_2 and Al_2O_3 layers, which we refer to as bilayers. Shown in Fig. 2 is a schematic cross section of a ZAO nanolaminate delineating total thickness, bilayer thickness, and individual layer thickness. Nanolaminates were deposited with bilayer thicknesses of 5, 10, and 20 nm. Nanolaminate compositions of roughly 25%, 50%, and 75% overall ZrO_2 content were synthesized by varying the thickness ratio of the ZrO_2 and Al_2O_3 layers in each bilayer. For example, a 200 nm thick, 10 nm bilayer, 75% ZrO_2 content ZAO laminate film would have a ZrO_2 layer thickness of approximately 7.5 nm, and an Al_2O_3 layer thickness of ap-

a)Author to whom correspondence should be addressed; electronic mail: jconley@eecs.oregonstate.edu

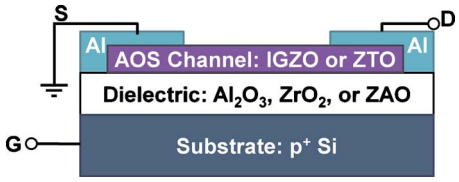

FIG. 1. (Color online) Schematic cross section of the staggered bottom-gate TFTs used in this study.

proximately 2.5 nm. In order to enhance the initial nucleation of ZrO_2 on the Si substrate for the nanolaminates that would begin with ZrO_2, depositions begin with an initial ten ALD cycles of Al_2O_3. For nanolaminates that begin with Al_2O_3, ten extra cycles of Al_2O_3 are added for consistency. The thickness of single layer ZrO_2 and Al_2O_3 films was measured using a spectroscopic ellipsometer. The thickness of individual layers in nanolaminates was estimated from the experimentally determined ALD deposition rates of Al_2O_3 ($\sim$0.089 nm/cycle) and ZrO_2 ($\sim$0.079 nm/cycle).

Following deposition of the gate oxide, an approximately 60 nm thick AOS channel layer of either ZTO or IGZO was deposited via rf magnetron sputtering at a pressure of 5 mTorr in a 90/10 Ar/O_2 atmosphere. No additional clean was performed between the gate dielectric deposition and AOS channel deposition. A shadow mask was used to define active regions of 100 μm in length and 1000 μm in width, giving a W/L ratio of 10. ZTO was deposited in an AJA Orion V using a 3 in. ZTO target (AJA) and a rf power of 100 W. IGZO was deposited using a custom-built sputtering system with a 3 in. IGZO target (Cerac) and a rf power of 100 W. Following deposition, IGZO films were annealed at 300 °C for 1 h with a 2 °C/min ramp rate. ZTO films received a postdeposition annealing for 1 h at 400 °C with a 5 °C/min ramp rate. Finally, the SBG TFT structures were completed by thermally evaporating Al through a shadow mask to form source and drain contacts.

In addition to TFTs, metal-insulator-semiconductor (MIS) devices with 40 nm thick dielectrics were prepared on both lightly doped (12–15 Ω cm) and heavily doped (50–80 m Ω cm) p-type Si. Evaporated Al dots with nominal areas of 1.3×10^{-4}, 2.5×10^{-4}, and 5.1×10^{-4} form the top metal contact for the MIS devices.

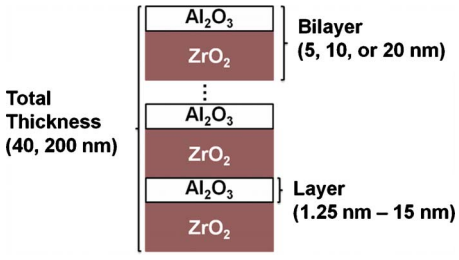

FIG. 2. (Color online) Schematic cross section of a ZAO nanolaminate illustrating the total thickness, bilayer thickness, and individual layer thickness. Overall ZrO_2 content is controlled simply by adjusting the ratio of individual layer thickness for each bilayer. In this example, 75% of the bilayer thickness consists of ZrO_2 and 25% consists of Al_2O_3, indicating an overall ZrO_2 content of 75%.

B. Electrical characterization

All electrical measurements were performed in a dark box in atmosphere at room temperature. Capacitance versus voltage (C-V) measurements (100 kHz) were performed on MIS structures with lightly doped Si substrates using an Agilent E4980A *LCR* meter. The relative dielectric constant (κ) of the dielectric stack was extracted from the slope of the accumulation capacitance versus device area. Current density versus field (J-ξ) measurements were performed on MIS structures with heavily doped Si substrates using an Agilent 4155B semiconductor parameter analyzer. Leakage current density and breakdown strength were extracted by grounding the back contact and sweeping the gate voltage in +100 mV increments at a sweep rate of approximately 200 mV/s until irreversible breakdown occurred.

Double-sweep I_D-V_{GS} transfer curves were taken on SBG TFTs using an Agilent 4155B with V_{DS} held at +1 V. One double-sweep consists of an initial hold time of 5 s, followed by ramping V_{GS} from +20 V to −5 V and then back to +20 V in 100 mV steps with a sweep rate of approximately 200 mV/s. To stabilize operation, a total of 5 double sweeps was performed. The fifth transfer curve was analyzed for V_{ON}, subthreshold swing (S), the I_{ON}/I_{OFF} ratio, hysteresis (ΔV_{hys}), and incremental electron mobility (μ_{inc}). V_{ON} was empirically defined as the onset of 1 nA of drain current in the $\log(I_D)$-V_{GS} transfer curve.[7,37] S was defined as the inverse maximum slope of the positive to negative sweep $\log(I_D)$-V_{GS} trace and is reported in units of mV/decade of current. I_{ON} current was measured at 10 V above V_{ON}, I_{OFF} was taken at V_D=−5 V; both were extracted from the positive to negative sweep $\log(I_D)$-V_{GS} trace so that I_{OFF} is fairly constant with respect to V_{GS}. ΔV_{hys} was extracted as the difference in V_{ON} between positive and negative sweeps. Following Hoffman,[37] μ_{inc} was extracted from I_D-V_{GS} curves using

$$\mu_{\text{inc}}(V_{GS}) = \lim_{V_{DS}\to 0}\left[\frac{\frac{\partial G_d(V_{GS})}{\partial V_{GS}}}{C_G\cdot\frac{W}{L}}\right], \tag{1}$$

where G_d is the channel conductance, C_G is the geometric capacitance of the gate oxide, and W and L are the width and length of the transistor. For each device, μ_{inc}, is reported at 10 V above V_{ON}. To assess device stability, long term bias stressing was performed with V_{GS}=+20 V and V_{DS}=+1 V. Stress was interrupted at approximately logarithmic time intervals to measure I_D-V_{GS} transfer curves.

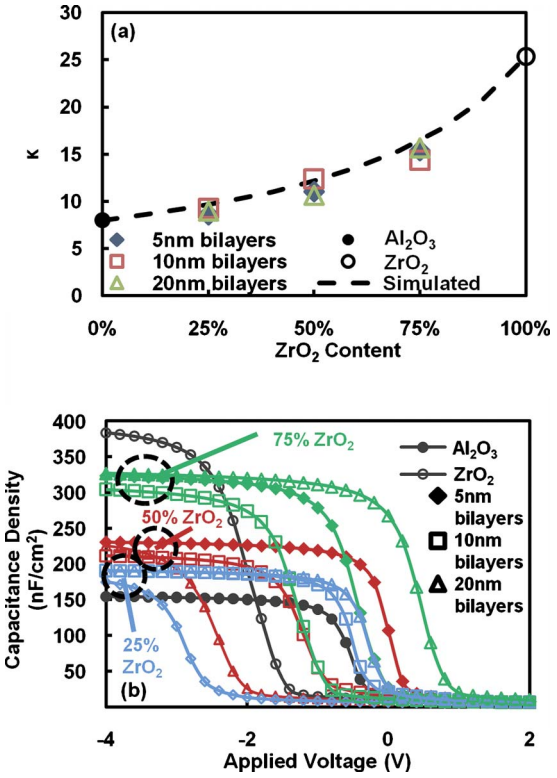

FIG. 3. (Color online) (a) Plot of κ vs overall ZrO_2 content for 200 nm thick ZAO nanolaminate films with 5, 10, and 20 nm thick bilayers. Single layer Al_2O_3 and ZrO_2 films are shown at ZrO_2 contents of 0% and 100%, respectively. The dashed line shows the simulated κ obtained by assuming a simple series combination of Al_2O_3 and ZrO_2 capacitors. (b) Representative capacitance vs voltage curves for the same devices.

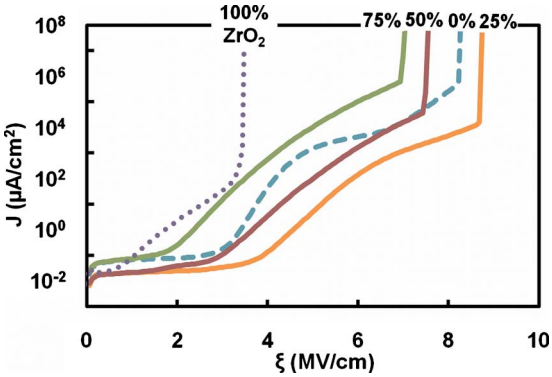

FIG. 4. (Color online) Representative plots of ramped J-ξ sweeps for a series of 40 nm thick ZAO nanolaminates with 5 nm bilayers and varying overall ZrO_2 content. The 40 nm thick single layer Al_2O_3 film is labeled 0% ZrO_2.

III. RESULTS AND DISCUSSION

A. MIS devices

Shown in Fig. 3(a) is a plot of the experimentally determined κ as a function of overall ZrO_2 content for 40 nm thick ZAO nanolaminate dielectrics with bilayer thicknesses (see Fig. 2) of either 5, 10, or 20 nm. Representative capacitance versus voltage curves are shown in Fig. 3(b). The single layer Al_2O_3 films (shown at 0% ZrO_2) and ZrO_2 films (100% ZrO_2) were found to have average κ values of 8.0 and 25.3, respectively. The average κ values for the ZAO nanolaminate films are bounded by these two extremes and increase with overall ZrO_2 content roughly as expected for a simple series combination of ZrO_2 and Al_2O_3 capacitors (shown as a dashed line). The bilayer thickness (or number of interfaces) does not appear to have a significant impact on κ, which is expected as previous studies have reported an impact of bilayer thickness only for bilayer thicknesses below ~2 nm.[30,38]

Shown in Fig. 4 are representative ramped current density versus electric field (ξ) plots for MIS devices with various dielectrics with the same physical thickness of 40 nm. For the ZAO nanolaminates, the bilayer thickness was fixed at 5 nm and composition was either 25%, 50%, or 75% overall ZrO_2 content. Single layer films showed an average breakdown strength of approximately 8 MV/cm for Al_2O_3 and approximately 3.4 MV/cm for ZrO_2. As expected, nanolaminate breakdown strength tended to decrease with increasing ZrO_2 content, with the exception of the 25% ZrO_2 content film, which showed an increased average breakdown strength over the single layer Al_2O_3. Bilayer thickness (not shown) did not have a strong impact on the average breakdown strength of the nanolaminates. The shape of the J-ξ curve is a function ZrO_2 content, indicating the dominance of different conduction mechanisms for the Al_2O_3, ZrO_2, and ZAO laminate films. For the 25% and 50% laminates, the conductive "knee" (the field at which the leakage slope increases but breakdown does not occur) occurs at higher fields than for the Al_2O_3 film whereas in the 75% ZrO_2 film, this "knee" occurs at a lower field. Because of this, the influence of ZrO_2 content on J is a function of ξ.

Shown in Fig. 5 are plots of the average current density (J_{AVG}) versus ZrO_2 content for the devices shown in Fig. 4, extracted at electric fields of (a) 1 MV/cm and (b) 4 MV/cm. Also included in Fig. 5 are data from ZAO nanolaminates with bilayer thicknesses of 10 and 20 nm. Once again, data points at 0% and 100% ZrO_2 content refer to single layer Al_2O_3 and ZrO_2 dielectrics, respectively. At low fields of 1–2 MV/cm, typical of TFT operation, J_{AVG} increases only weakly with increasing ZrO_2 content. Between the single layer Al_2O_3 films and the 75% ZrO_2 laminates, J_{AVG} increases by less than a factor of 2. Once again, bilayer thickness did not appear to have a strong effect.

At 4 MV/cm [Fig. 5(b)], the relationship between leakage current density and ZrO_2 content is more complex. In all cases, the 25% ZrO_2 content films exhibited much lower leakage than the single layer Al_2O_3 films. At 50% ZrO_2 content, both the 5 and 10 nm bilayer films still showed lower leakage than the single layer Al_2O_3 while the 20 nm bilayer films were slightly higher. It is not until the laminate films reach 75% ZrO_2 content that they all exhibit higher leakage than the single layer Al_2O_3 films. At 4 MV/cm, all of the single layer ZrO_2 films have experienced breakdown and therefore are not shown. Leakage current density at 4 MV/cm appears to be a weak function of bilayer thickness, trending higher with increasing bilayer thickness. This may

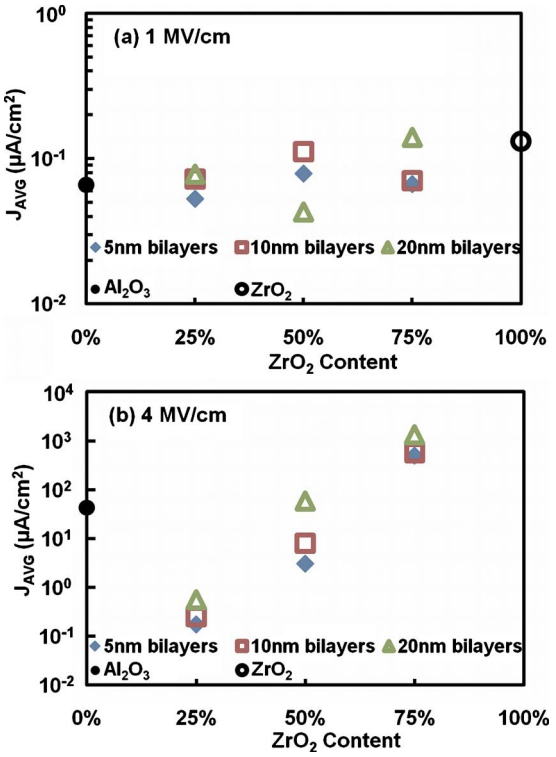

FIG. 5. (Color online) Plot of average leakage current density (J_{AVG}) vs overall ZrO_2 content for 40 nm thick ZAO nanolaminates with bilayer thicknesses 5, 10, and 20 nm at electric fields of (a) 1 MV/cm and (b) 4 MV/cm. Also shown are the leakage current density values for 40 nm thick single layer films of Al_2O_3 (at 0% ZrO_2) and ZrO_2 (at 100% ZrO_2).

be caused by the larger crystal grains in thicker ZrO_2 layers, which grow until terminated with an Al_2O_3 layer, increasing the roughness of the films.[39]

B. TFTs

The possibility of increased C_{ox} with little leakage current penalty suggests that these nanolaminates may offer advantages as gate dielectrics for TFTs. The details of the dielectric-channel interface are known to play an important role in determining the performance and stability of field-effect devices. Nanolaminate films can be terminated with a final layer of either Al_2O_3 or ZrO_2 to form the interface with the AOS channel. Shown in Fig. 6 are I_D-V_{GS} transfer curves and I_G-V_{GS} curves for IGZO and ZTO channel TFTs with 200 nm thick, 10 nm bilayer ZAO laminate dielectrics terminating with either Al_2O_3 (5 nm ZrO_2/5 nm Al_2O_3/AOS channel) or ZrO_2 (5 nm Al_2O_3/5 nm ZrO_2/AOS channel) at the AOS channel interface. Since the overall composition is the same, all of these dielectrics have the same dielectric constant. Relevant parameters of these devices are tabulated in Table I. For IGZO channel TFTs with ZAO laminate dielectrics, Al_2O_3/IGZO interface devices show improved characteristics as compared to ZrO_2/IGZO interface devices, including increased μ_{inc}, reduced ΔV_{hys}, and reduced S. For the ZTO TFTs with nanolaminate dielectrics, the benefits are

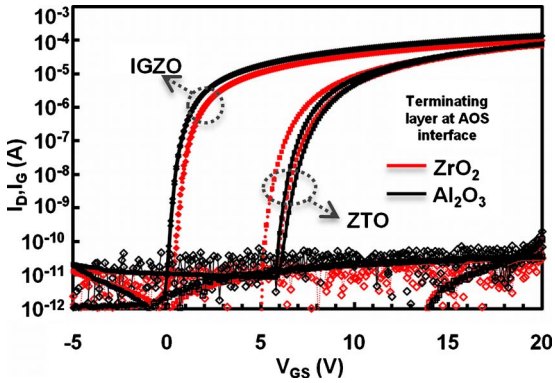

FIG. 6. (Color online) Plot of I_D-V_{GS} and I_G-V_{GS} for IGZO and ZTO TFTs with 200 nm thick ZAO dielectrics composed of 10 nm bilayers and 50% overall ZrO_2 content, with either Al_2O_3 or ZrO_2 termination at the AOS interface.

not as clear. Devices with Al_2O_3/ZTO interfaces showed reduced ΔV_{hys} and increased μ_{inc}, but increased S as compared to ZrO_2/ZTO devices.

The data from Figs. 3–5 suggest that some laminate compositions may allow improved performance over single layer dielectrics for TFT applications. Shown in Fig. 7 are I_D-V_{GS} transfer curves and I_D-V_{GS} plots for IGZO channel TFTs with 200 nm thick gate dielectrics of either single layer ZrO_2, single layer Al_2O_3, or 10 nm bilayer ZAO nanolaminates of 25%, 50%, and 75% ZrO_2 content. All devices except the single layer ZrO_2 have an Al_2O_3/IGZO interface. Relevant parameters of these devices are tabulated in Table II. While the single layer ZrO_2 dielectric devices have significantly higher I_G than the rest of the devices, there appears to be no significant difference in I_G between devices with ZAO nanolaminates and single layer Al_2O_3 dielectrics. This result is consistent with the weak dependence of 1 MV/cm leakage current density on ZrO_2 content seen for the 40 nm thick nanolaminate MIS devices [Fig. 5(a)]. Looking first at the performance parameters of TFTs with single layer dielectrics, the ZrO_2 gate dielectric devices showed high I_{ON} and the lowest S (both due in part to having the largest capacitance), medium ΔV_{hys} and μ_{inc}, but the worst I_{OFF} and thus the worst I_{ON}/I_{OFF} ratio. The single layer Al_2O_3 dielectric devices exhibited lower I_{OFF} than the ZrO_2 devices, but also lower I_{ON} and higher S (due in part to the lower capacitance), lower μ_{inc}, and the largest ΔV_{hys} of any of the devices. For the TFTs with ZAO laminate dielectrics, the 25% ZrO_2 dielectric devices had low I_{OFF}, excellent I_{ON}/I_{OFF}, and good I_{ON}, but also the worst S and worst μ_{inc} of any of the devices. The 50% ZrO_2 dielectric devices had the lowest I_{OFF}, the best I_{ON}/I_{OFF}, and the lowest ΔV_{hys}, but only medium μ_{inc}. Finally, the 75% ZrO_2 content dielectric devices had good I_{ON}/I_{OFF}, very low ΔV_{hys}, medium substhreshold slope, and the highest μ_{inc}. For the nanolaminate dielectric devices, V_{ON} decreased, I_{OFF} increased, and μ_{inc} increased with increasing overall ZrO_2 content. Devices with ZAO nanolaminate dielectrics accounted for the best I_{OFF}, highest I_{ON}, lowest ΔV_{hys}, and highest μ_{inc}. Overall the 75% ZrO_2 content laminate (7.5 nm ZrO_2/2.5 nm Al_2O_3 bilayer structure) was the

TABLE I. Comparison of device parameters for ZTO and IGZO TFTs with 200 nm thick ZAO dielectrics composed of 10 nm bilayers with 50% overall ZrO_2 content (5 nm Al_2O_3/5 nm ZrO_2), terminated with either 5 nm Al_2O_3 or 5 nm ZrO_2 at the AOS interface.

Nanolaminate/AOS interface	μ_{inc} (cm^2/V s)	S (mV/dec)	ΔV_{hys} (V)	I_{ON}/I_{OFF}	κ
ZrO_2/Al_2O_3/IGZO	14.2	131	0.01	10^8	12.4
Al_2O_3/ZrO_2/IGZO	10.65	158	0.04	10^8	12.4
ZrO_2/Al_2O_3/ZTO	15.4	260	0.39	9×10^6	12.4
Al_2O_3/ZrO_2/ZTO	13.6	226	0.85	9×10^6	12.4

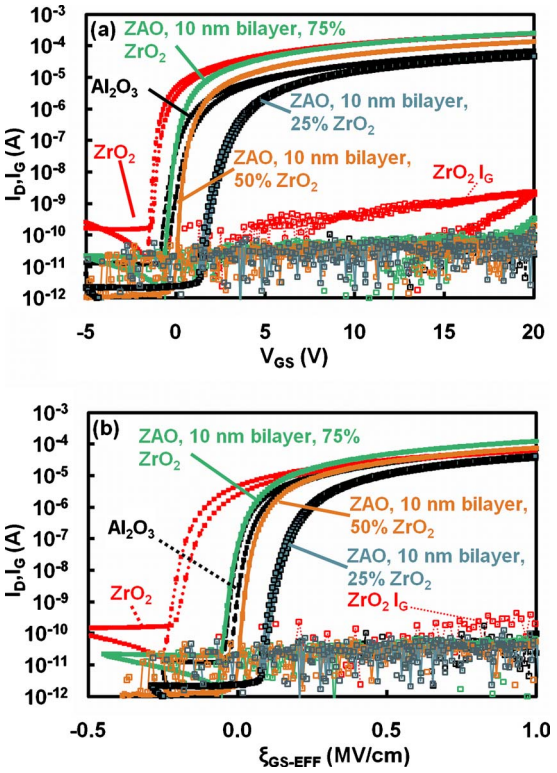

FIG. 7. (Color online) (a) Plot of I_D-V_{GS} transfer curves and I_G-V_{GS} gate leakage characteristics for IGZO TFTs with 200 nm thick gate dielectrics consisting of either Al_2O_3, ZrO_2, or 10 nm bilayer ZAO laminates of 25%, 50%, and 75% overall ZrO_2 content. (b) Plot of I_D-$\xi_{GS\text{-}EFF}$ and I_G-$\xi_{GS\text{-}EFF}$ for the same data with effective electric field normalized to the capacitive equivalent thickness of Al_2O_3.

best performing dielectric for the IGZO TFTs in this study, indicating that nanolaminate films may be able to combine the benefits of both component dielectrics to produce better performance than either of the single layer films.

Note that because of varying composition and κ, each of the 200 nm thick dielectrics have different capacitances and thus, for the same applied V_{GS}, will induce different charge densities in the AOS channel. In order to account for this difference, we use the concept of capacitive equivalent thickness (CET) in which the thickness of each film is normalized to a capacitive equivalent thickness of Al_2O_3. The CET of a dielectric is defined as $\text{CET}=d_{phys}\times(\kappa_{Al_2O_3}/\kappa_{dielectric})$, where d_{phys} is the physical thickness of the dielectric (in all cases 200 nm) and $\kappa_{dielectric}$ is the κ of the dielectric for which we are calculating the CET. Using the CET for each dielectric, the effective gate electric field, $\xi_{GS\text{-}EFF}=\xi_{GS}/\text{CET}$, required to generate a given charge density in the channel can be determined. Shown in Fig. 7(b) are the data from Fig. 7(a) replotted against $\xi_{GS\text{-}EFF}$. It is seen that when the differences in capacitance are accounted for, the high capacitance dielectrics such as ZrO_2 look a bit worse (increased S and decreased I_{ON}) while the single layer Al_2O_3 device looks a bit better (reduced S and increased I_{ON}). The conclusions drawn from Fig. 7(a) remain the same, however, in that the 50% and 75% content 10 nm bilayer laminates still exhibit the best overall performance.

An important consideration for commercial applications of AOS TFTs is operational stability.[14–18] Shown in Fig. 8 are plots of ΔV_{ON} versus dc bias stress time for IGZO TFTs with 200 nm thick gate dielectrics consisting of either single layer Al_2O_3, ZrO_2, or ZAO laminates with a variety of bilayer structures. All devices have an Al_2O_3/IGZO interface. All devices were stressed using the same conditions: V_{GS}= +20 V (ξ_{GS}=+1 MV/cm) with V_{DS}=1 V. Stress was inter-

TABLE II. Comparison of device parameters for IGZO TFTs with 200 nm thick gate dielectrics of Al_2O_3, ZrO_2, or 10 nm bilayer ZAO laminates of 25%, 50%, and 75% overall ZrO_2 content.

Dielectric or bilayer structure (nm)	μ_{inc} (cm^2/V s)	S (mV/dec)	ΔV_{hys} (V)	I_{ON}/I_{OFF}	κ
Al_2O_3	12.0	151	0.45	6×10^6	8.0
2.5 ZrO_2/7.5 Al_2O_3	7.2	247	0.24	2×10^7	9.3
5.0 ZrO_2/5.0 Al_2O_3	14.2	131	0.01	10^8	12.4
7.5 ZrO_2/2.5 Al_2O_3	22.3	152	0.02	10^7	14.4
ZrO_2	16.1	100	0.19	2×10^6	25.3

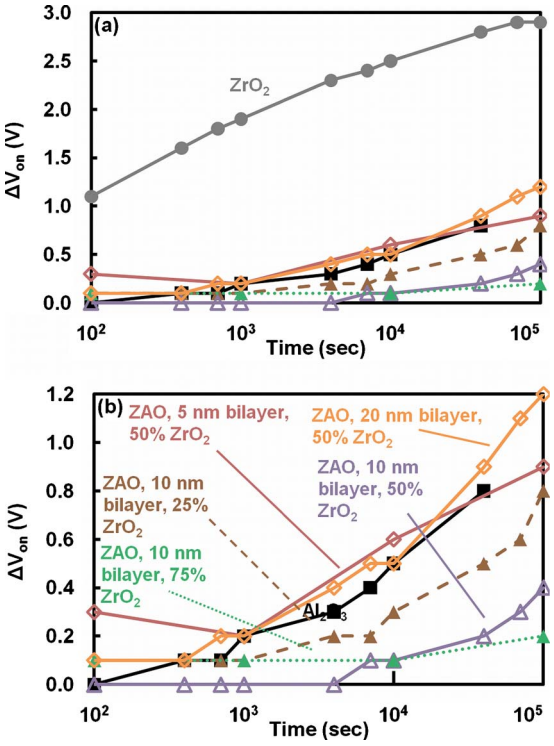

FIG. 8. (Color online) (a) Plot of ΔV_{ON} vs positive dc bias stress time for IGZO TFTs with a variety of 200 nm thick gate dielectrics. (b) Same data with *y*-scale zoomed in to focus on ΔV_{ON} shifts in Al_2O_3 and nanolaminate gate dielectric devices.

rupted at regular time intervals to measure I_D-V_{GS} transfer curves. Because I_D-V_{GS} transfer curves took about 10^2 s to collect, Fig. 8 begins at an accumulated bias stress time of 10^3 s. Devices with a single layer Al_2O_3 dielectric showed ΔV_{ON} of roughly 0.8 V at 2×10^4 s. As seen in Fig. 8(a), ΔV_{ON} was the worst in devices with single layer ZrO_2. Shown in the zoomed *y*-axis scale plot in Fig. 8(b), it is seen that the bias stress performance of the 5 and 20 nm thick bilayer laminates was comparable to single layer Al_2O_3. All of the 10 nm bilayer ZAO nanolaminate films, regardless of ZrO_2 content, performed as well or better than single layer Al_2O_3, exhibiting lower ΔV_{ON} at long stress times. Once again, the 75% ZrO_2 10 nm bilayer ZAO performed the best with only a 0.2 V shift after 10^5 s of stress.

As seen in Fig. 8, TFTs with single layer ZrO_2 dielectrics suffer more from ΔV_{ON} than TFTs with single layer Al_2O_3 dielectrics. Much of this is likely due to the different chemical natures of the IGZO/AOS and Al_2O_3/AOS interfaces. In addition, the increased susceptibility of ZrO_2 to positive gate bias stress may be due in part to the smaller conduction band offset of ZrO_2 to IGZO, which allows more injection into the ZrO_2 layer (see Figs. 4 and 5), which in turn leads to increased electron trapping and increased ΔV_{ON} as compared to single layer Al_2O_3. The presence of Al_2O_3 at the interface, which has a larger conduction band offset to IGZO, may help in preventing electrons from being injected into the ZrO_2 layer and thus lead to a reduction in ΔV_{ON} as a function of stress time. What is puzzling is the observation in Fig. 7 that TFTs with laminate Al_2O_3 interfaces can perform better than single layer Al_2O_3 interfaces. That is, the use of a thin Al_2O_3 layer at the interface can in some cases perform better than a thick single layer Al_2O_3 dielectric. Combined with the stability results from Fig. 8, this suggests that there may be an optimal thickness for the near-interfacial bilayer structure to attain the best overall performance and stability. Although there is no clear overall dependence of ΔV_{ON} on the Al_2O_3 interfacial layer thickness, ΔV_{ON} for the 10 nm bilayer nanolaminates appears to become larger as the thickness of the Al_2O_3 layer at the AOS interface increases. During sputter deposition of the AOS channel, the surface of the dielectric is exposed to energetic particle bombardment from the plasma, which could create traps in the dielectric. Al_2O_3 may be more susceptible to this damage than ZrO_2. As a result, the use of an Al_2O_3 interfacial layer that is thicker than necessary to impede charge injection (order of a few nanometers) may lead to a larger ΔV_{ON} than a thinner Al_2O_3 interfacial layer, due the creation of additional traps near the dielectric/channel interface. It therefore may be possible to optimize the bilayer structure with the interfacial Al_2O_3 layer effectively arranged so as to suppress the electron injection into the ZrO_2 layer while at the same time avoiding excessive plasma-induced electron traps. It is likely that the optimum arrangement of the interfacial bilayer will be a function of the AOS material (interface chemistry) as well as the processing details of the AOS deposition.[19]

IV. SUMMARY AND CONCLUSIONS

ZrO_2–Al_2O_3 nanolaminate dielectrics consisting of a series of ZrO_2–Al_2O_3 bilayers were deposited via ALD with various bilayer thicknesses. The percentage of ZrO_2 in the laminates was varied by adjusting the ratio of ZrO_2 layer thickness to Al_2O_3 layer thickness within each ZrO_2–Al_2O_3 bilayer. The relative dielectric constants of ZAO laminate films in MIS devices were found to be between those of single layer ZrO_2 and single layer Al_2O_3 films, increasing with increasing ZrO_2 content as would be expected from a simple series of Al_2O_3 and ZrO_2 capacitors. Leakage current density was found to be a function of ZrO_2 content as well as the applied electric field. At low electric fields, in the range suitable for TFT operation (1–2 MV/cm), leakage current density increased only weakly with increasing ZrO_2 content. At higher fields (~4 MV/cm), nanolaminate films with 25% and 50% ZrO_2 had lower leakage currents than single layer Al_2O_3 films. Neither the relative dielectric constant nor leakage was found to be a strong function of bilayer thickness.

ZAO nanolaminates were used as gate dielectrics for IGZO and ZTO TFTs. It was found that terminating ZAO laminate dielectrics with a layer of Al_2O_3, so as to provide an Al_2O_3/AOS channel interface rather than a ZrO_2/AOS channel interface, resulted in improved device characteristics for IGZO channel devices. In addition, it was found that ZAO nanolaminate dielectrics could be engineered to outperform the constituent single layer dielectrics for AOS TFT applications, providing improved TFT performance and stability.

For IGZO TFTs, both 50% and 75% ZrO_2 content 10 nm bilayer films showed better performance than single layer Al_2O_3 films with μ_{inc} as high as 22.3 cm^2/V s, low ΔV_{hys}, and minimal ΔV_{ON} during extended positive dc bias stressing. For 10 nm bilayer array, ΔV_{ON} appears to decrease as the thickness of the Al_2O_3 interfacial layer decreases. However, the lack of a universal dependence of device performance on the thickness of the Al_2O_3 interfacial layer in all laminate films suggests that there may be an optimum thickness that depends not only on the AOS material but also on the trade-off between the effectiveness of Al_2O_3 as a barrier to electron injection and the susceptibility of Al_2O_3 to sputter damage, the thickness of the adjacent ZrO_2 layer, and/or the deposition details of the AOS material.

ACKNOWLEDGMENTS

This work was supported in part by grants from the National Science Foundation (through Grant No. DMR-0805372 and an REU supplement) and matching funds from the Oregon Nanoscience and Microtechnologies Institute (ONAMI). The authors thank Professor Greg Herman (OSU ChE) for the ZTO used in this study.

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